	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
1	BRS	L1	0	yrh near fang-yu.in.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/28 16:57	
2	BRS	L2	323	lin near chi.in.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/28 17:02	
3	BRS	L3	1	chen near chuang-hsiang.in.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/28 17:02	

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
4	BRS	L4	63	439/197.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/28 17:03	
5	BRS	L5	925	438/197.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/28 17:08	
6	BRS	L6	6251	(substrate) near25 (gate near dielectric)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/28 17:09	

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
7	BRS	L7	1637	(substrate) near25 (gate near dielectric) near25 (conductive or polysilicon)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/28 17:10	
8	BRS	L8	205	(substrate) near25 (gate near dielectric) near25 (conductive or polysilicon) near25 (opening or trench or via or recess)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/28 17:11	
9	BRS	L9	3829	(substrate) near25 (dielectric) near25 (conductive or polysilicon) near25 (opening or trench or via or recess)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/28 17:11	

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
10	BRS	L10	392	(substrate) near25 (dielectric) near25 (conductive or polysilicon) near25 (opening or trench or via or recess) near35 (mask or photoresist or resist)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/28 17:56	
11	BRS	L11	98	(substrate) near25 (silicon near oxide) near25 (conductive or polysilicon) near25 (opening or trench or via or recess) near35 (mask or photoresist or resist)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/28 17:57	
12	BRS	L12	43	(substrate) near25 (silicon near oxide) near25 (conductive or polysilicon) near25 (opening or trench or via or recess) near35 (mask or photoresist or resist) near35 (remov$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/28 19:12	

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
13	BRS	L13	270	(source/drain) near25 (substrate) near25 (remov$3 near15 mask)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/28 18:25	
14	BRS	L15	1	(source/drain) near25 (substrate) near25 (well) near25 (remov$3 near15 implantat$3 near3 mask)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/28 18:26	
15	BRS	L14	17	(source/drain) near25 (substrate) near25 (well) near25 (remov$3 near15 mask)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/28 18:32	

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
16	BRS	L16	48	(source and drain) near25 (substrate) near25 (well) near25 (remov$3 near15 mask)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/28 18:53	
17	BRS	L17	1	(source and drain) near25 (substrate) near25 (well) near25 (remov$3 near15 mask) near35 (anti or reflect$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/28 18:39	
18	BRS	L18	640	(anti-reflection) near25 (mask)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/28 18:39	

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
19	BRS	L19	412	(etch$3 or pattern$3) near25 (anti-reflection) near25 (mask)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/28 18:40	
20	BRS	L20	110	(etch$3 or pattern$3) near25 (anti-reflection) near25 (mask) near25 (opening or via or hole or recess or trench or aperture)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/28 18:41	
21	BRS	L21	7898	(refractory metal near silicide) near15 (conductive)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/28 19:04	

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
22	BRS	L22	780	(refractory near metal near silicide) near15 (conductive)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/28 19:04	
23	BRS	L23	3	(refractory near metal near silicide) near15 (conductive) near15 (tungsten and nickel)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/28 19:05	
24	BRS	L24	112	(refractory near metal near silicide) near15 (conductive) near15 (tungsten or nickel)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/28 19:06	

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
25	BRS	L25	6	(refractory near metal near silicide) near15 (conductive) near15 (tungsten or nickel) near15 (substrate)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/28 19:06	
26	BRS	L26	47	(inter-layer near dielectric) near15 (substrate) near15 (opening)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/28 19:13	
27	BRS	L27	1	(inter-layer near dielectric) near15 (substrate) near15 (opening) near25 (mask)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/28 19:13	

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
28	BRS	L28	553	(dielectric) near15 (substrate) near15 (opening) near25 (mask)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/28 19:13	
29	BRS	L29	4	(dielectric) near15 (substrate) near15 (opening) near25 (self-aligned near mask)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/28 19:14	
30	BRS	L30	0	(substrate) near15 (opening) near25 (cap) near15 (self-aligned near mask)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/28 19:15	

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
31	BRS	L31	0	(substrate) near15 (hole or via or recess or aperture or trench) near25 (cap) near15 (self-aligned near mask)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/28 19:15	
32	BRS	L32	0	(substrate) near15 (sti) near25 (cap) near15 (self-aligned near mask)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/28 19:15	
33	BRS	L33	25	(substrate) near15 (hole or via or recess or aperture or trench) near25 (self-aligned near mask)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/10/28 19:16	

	U	1	Document ID	Title	Current OR	Pages
1	☐	☐	US 20040207024 A1	Semiconductor device with an STI structure which is capable of suppressing inverse narrow channel effect, and method of manufacturing the same	257/374	17
2	☐	☐	US 20040159879 A1	Non-volatile semiconductor memory device and manufacturing method of the same	257/315	18
3	☐	☐	US 20040094807 A1	Tri-gate devices and methods of fabrication	257/401	20
4	☐	☐	US 20040036127 A1	Tri-gate devices and methods of fabrication	257/401	27
5	☐	☐	US 20040036126 A1	Tri-gate devices and methods of fabrication	257/401	20
6	☐	☐	US 20020031882 A1	METHOD FOR MANUFACTURING A SEMICONDUCTOR INTEGRATED CIRCUIT OF TRIPLE WELL STRUCTURE	438/228	26

	U	1	Document ID	Title	Current OR	Pages
7	☐	☐	US 6531363 B2	Method for manufacturing a semiconductor integrated circuit of triple well structure	438/275	26
8	☐	☐	US 6127226 A	Method for forming vertical channel flash memory cell using P/N junction isolation	438/259	14
9	☐	☐	US 5628871 A	Method of removing resist mask and a method of manufacturing semiconductor device	438/514	14
10	☐	☐	US 5393679 A	Use of double charge implant to improve retrograde process PMOS punch through voltage	438/217	9
11	☐	☐	US 5296394 A	Manufacturing method of GaAs metal semiconductor FET	438/81	5

	U	1	Document ID	Title	Current OR	Pages
12	☐	☐	US 20040159879 A	Non-volatile semiconductor memory device comprises memory cell having gate insulating film, floating gate, insulating film, control gate and pair of source/drain region		18
13	☐	☐	US 20040087075 A	Formation of metal oxide semiconductor field effect transistor or complementary metal oxide semiconductor device on semiconductor substrate comprises forming gate insulator having high-dielectric constant dielectric layer		18
14	☐	☐	US 6656764 B	Formation of metal oxide semiconductor field effect transistor device comprises removing hard mask resulting in space between lightly doped source/drain polysilicon spacers and forming gate insulating layer in space		16
15	☒	☐	TW 477038 A	Local ion implantation method for forming a twin well structure - uses the same photo mask to form the well and channel		1

	U	1	Document ID	Title	Current OR	Pages
16	☒	☐	US 5393679 A	Semiconductor CMOS device mfr. on silicon@ substrate doped with N-dopant - comprises forming P-well mask on substrate, implanting dopant ions, performing NMOS first implant of ions into substrate, removing P-well mask, etc.		9
17	☒	☐	TW 237563 A	Process for static random access device - with buried layer structure		NA